



# 2027 SPARC<sup>1</sup> Solicitation for SRC Projects Program

## Application Guidance Document<sup>2</sup>

**Funding Opportunity Title:** 2027 SRC SPARC Projects Solicitation

**Funding Opportunity Number:** SPARC-SPP-2027

**Release Date:** 06/02/2026

## Key Dates

Activity/Event	Date
Project Solicitation Opens	06/02/2026
Concept Paper Round Closes	06/30/2026
Proposal Round Opens	08/03/2026
Proposal Round Closes	09/14/2026
Target Project Start	01/01/2027

The SRC SPARC Projects Program, operated by the Semiconductor Research Corporation (SRC) as part of SRCco, is an industry-driven, precompetitive research program advancing global leadership in semiconductor innovation through collaborative, industry member-directed academic research.

Please note that all details are subject to change without notice.

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<sup>1</sup> Semiconductor and Packaging Advanced Research Consortium

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## Executive Summary

### **Concise Description of Program and Funding Opportunity**

The SPARC (Semiconductor and Packaging Advanced Research Consortium) Projects Program is an SRC operated, industry funded and directed program for sponsoring member driven pathfinding through collaborative academic research. SPARC is structured as a project-based program enabling members to directly define research priorities and guide selection of proposed projects. The framework allows members to engage closely with principal investigators through SRC's proven governance and IP framework. Projects are organized into Technical Tracks, each having 1-3 projects, and executed as multi-year collaborative efforts that produce tangible insights and outputs such as data, models, code, samples, process recipes, research approaches, and experimental results, while strengthening the semiconductor talent pipeline through direct student involvement and hiring.

### **Solicitation Description:**

This is a collaborative, two-round solicitation process. The first round requires submission of a concept paper. Selected concept papers will be invited to submit full proposals in the second round. Detailed information on both rounds is provided within this document.

Interested Principal Investigators (PIs) may submit a two-page Concept Paper describing their proposed approach to addressing the listed technical topics. Concept Papers will be reviewed by industry technical experts, and selected PIs will be invited to submit Full Applications. Full Applications will then be evaluated using the rating criteria provided later in this document, with final selections based on proposal quality, portfolio balance, and alignment with sponsoring members' interests. Interested PIs are encouraged to carefully review this document and ensure their Concept Papers and Full Applications are aligned with the interests of the sponsoring members.

### **Eligibility**

SPARC Technical Track proposals must include one (1), two (2), or three (3) distinct but coordinated projects that collectively address a common Technical Topic through complementary or integrated research efforts. Each project must identify a Project Lead, and the Track Lead must be one of these Project Leads, serving as the overall coordinator across all projects within the Technical Track. University research professors from all countries are eligible to submit proposals, except those in [Group D and E countries](#) , unless those countries are also designated as Group A or Group B.



**Priority Technical Topics**

This solicitation addresses 3 Technical Topics including:

1. **Analog & Mixed-Signal Technology & Design**
2. **Advanced Packaging**
3. **Manufacturing & Device Technology**

**Anticipated Amounts**

All projects will be conducted over a three-year period. Individual award amounts will be allocated at the amounts outlined below, with total SRC program funding expected to be between \$12M and \$15M.

Projects Per Technical Track	Per Year	3- year Award Value (excluding cost-share)
1 Project	\$150K	\$450K total
2 Projects	\$300K	\$900K total
3 Projects	\$450K	\$1.35M total

*Note: A proposal is a Technical Track inclusive of 1-3 projects.*

**Solicitation Definitions**

**Program:** A group of Technical Tracks with a common membership.

- **Example:** SPARC

**Technical Track:** A group of Projects managed by a Track Lead (TL) which is a university professor. Proposals, if selected, become a Technical Track.

- **Example:** *Packaged Transistors Heat Flow Modeling, led by Prof. Hall at Northbridge University*

**Track Lead:** The Track Lead is one of the Project Leads that is responsible for coordinating all projects within a Technical Track, ensuring coordination and alignment with the track’s technical objectives and managing collaboration among Project Leads.

**Project Lead (Principal Investigator, PI):** The professor responsible for leading and managing a Project, including oversight of all associated Tasks and deliverables.

**Project:** A group of Tasks aimed at delivering defined research outcomes, managed by a single Project Lead (PI). A Track Lead also serves as a Project Lead within their Technical Track.

- **Example:** *Thermal Analysis Through Borosilicate Glass Substrates*

**Tasks:** Discrete units of work that produce specific deliverables such as reports, data, algorithms/code, or prototypes resulting from the Project’s research.

- **Example:** *Provide thermal characterization measurements on Borosilicate Substrates by the end of Year 1; deliver a pathway to increase Kth on glass substrates by the end of Year 2; provide thermal modeling by the end of Year 3*



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# 1. SRC Projects Solicitation Topics

## 1.1 Solicitation Background

The SPARC (Semiconductor and Packaging Advanced Research Consortium) Projects Program is an SRC operated, industry funded and directed program for sponsoring member driven pathfinding through collaborative academic research. SPARC is structured as a project-based program enabling members to directly define research priorities and guide selection of proposed projects. The framework allows members to engage closely with principal investigators through SRC's proven governance and IP framework. Projects are organized into Technical Tracks, each having 1-3 projects, and executed as multi-year collaborative efforts that produce tangible insights and outputs such as data, models, code, samples, process recipes, research approaches, and experimental results, while strengthening the semiconductor talent pipeline through direct student involvement and hiring.

This SPARC solicitation builds on this foundation by translating member-defined research priorities into a focused set of Technical Topics that address key industry needs for the years ahead. The solicitation has been developed collaboratively with industry members to define the objectives, technical scope, and evaluation criteria that will ensure strong alignment with roadmap priorities and members' interests. It is being released through SRC's standard solicitation process, beginning with an open call for concept papers followed by a structured down-selection to invited full proposals. The goal of the solicitation is to attract high-quality, collaborative proposals that may span multiple institutions and disciplines, enabling the formation of cohesive Technical Tracks with sufficient scale and impact. Through this process, SPARC aims to create a balanced portfolio of projects that deliver measurable technical advances, maintain strong industry relevance, and provide members with clear influence over research direction and outcomes.

The objectives of this solicitation are to:

- Align research to common interests of members
- Develop technology that transfers into member companies
- Train/educate students to prepare for the semiconductor workforce, esp. grad students
- Enable the recruitment of talented students into SRC member companies

The goals of this solicitation are:

- Co-sponsorship of proposals by members to ensure maximum leverage of members' dues
- Identify and test emerging technology, especially within growing markets
- Make project- based research complimentary to center-based research
- Encourage faculty collaboration to achieve outcomes beyond individual efforts
- Attract new ideas from faculty not traditionally involved in SRC-funded research

In addition, as the semiconductor field enters a transformative era shaped by rapid advances in artificial intelligence (AI), we strongly encourage the research community to thoughtfully and proactively integrate practical AI into the core of their work, spanning research methodologies, design and modeling tools, experimental processes, communication, project

management and educational approaches. The objective is not to compete with commercial entities in the near-term commercialization of AI technologies, but rather to leverage AI as a powerful enabler of discovery, productivity, and insight to accelerate progress and improve efficiency across the semiconductor research stack while preparing the next generation of talent to operate at the intersection of physical and digital innovation. Proposals that demonstrate meaningful and reasonable incorporation of AI to enhance foundational research, improve system-level understanding, drive future generations of hardware advancements, and expand the effectiveness of teaching and workforce development will be especially well aligned with the goals of this solicitation.

## 1.2 Project Collaboration

This solicitation preserves SPARC's (SRC) project-based structure by allowing submissions as either single projects or collaborative efforts involving two or three projects. Maintaining this structure is essential to the program's objectives, while recognizing that small-scale collaborations can, in some cases, more effectively address defined technical objectives and provide broader technical coverage.

While not required for collaborative proposals, faculty with an established history of SRC engagement are encouraged to partner with researchers who have had limited or no prior SRC funding. This approach helps introduce new perspectives, expand the pool of contributors, and bring fresh ideas and thought leadership into the SRC ecosystem.

Collaborative proposals must clearly define roles and responsibilities across projects, including the coordination of responsibilities of the Track Lead. Proposals should include a plan for integration of project outcomes, identification of key technical interfaces and dependencies, and definition of joint track-level deliverables. Collaboration mechanisms, such as regular technical meetings, shared reviews, and coordinated reporting, must be described. Proposals are encouraged to include cross-institution and cross-disciplinary participation and should demonstrate how industry engagement and student collaboration will occur across the full Technical Track. Governance and decision-making processes, including conflict resolution and alignment of priorities, should also be addressed.

## 1.3 Solicitation Project Summary

Strong proposals will focus on exploratory, fundamental, or applied research at early stages of technological maturity, well before industry's development phase, with the goal of identifying and validating promising research pathways. This is especially relevant in high-growth and dynamic semiconductor areas such as AI inference, efficient infrastructure, smart autonomous systems, and devices.

### Proposal Details

Key proposal details are described below:

1. Project Budgets over a 3-year period (\$150K/project per year) not including cost share should be:
  - 1 Project - \$450K
  - 2 Projects - \$950K
  - 3 Project - \$1.35M



2. Cost-share Requirements
  - All Projects must have a minimum 20% cost-share which also includes in-kind.
3. Period of Performance
  - All projects will adhere to a 3-year period having an annual review and renewal.

#### **Required Deliverables**

Proposals must clearly define specific, measurable deliverables that will be produced over the duration of the project. Deliverables should reflect SPARC's emphasis on practical, high-impact outputs, and may include data sets, models, algorithms, design tools, experimental results, prototypes, processes, equipment, metrology or other artifacts that demonstrate the feasibility of technical progress with commercial impact beyond traditional publications. Over a 3-year period, two to five major milestones should be explicitly linked to the project's objectives and technical approach, ensuring that the work produces outcomes that are relevant, usable, and transferable to industry stakeholders.

Proposers are required to structure deliverables as a time-phased work plan, typically aligned with annual milestones. Deliverables should be clearly defined for each year of the project, including expected content, level of maturity, and how progress will be evaluated. Wherever possible, deliverables should support integration and collaboration across projects within a Technical Track, enabling broader impact than a single project alone. The clarity, completeness, and feasibility of the proposed deliverables will be a key factor in proposal evaluation. The proposal should identify which items of the Technical Topics are being addressed and what progress can be expected through the duration of the project.

### 1.4 Technical Topics

This solicitation addresses 3 Technical Topics including:

1. **Analog & Mixed-Signal Technology & Design**
2. **Advanced Packaging**
3. **Manufacturing & Device Technology**

Each of these Technical Topics has subtopics as described below. Additionally, a section on background, gaps, constraints, and challenges has been added below each topic area. This section should be used as guidance and is not expected to be exhaustive, limiting, or prescriptive. Proposers are encouraged to use their domain and industry knowledge to propose ideas that solve the problems and create opportunities for program members from the subtopics of their interest.

#### 1.4.1 Topic 1: Analog & Mixed-Signal Technology & Design

##### **Subtopics of Interest:**

- Analog & Mixed-Signal (AMS) Processing
- Design for Cryogenic Environments
- Power management, distribution, and power electronics
- RF-to-THz devices, circuits, & systems
- Photonics devices, materials, components

- Quantum Transduction
- Sensor innovations & Physical AI
- Magnetics and other passives

### **Background Gaps, Constraints, and Challenges Addressed**

As the semiconductor industry shifts from the traditional PC/mobile era toward AI-driven platforms, autonomous and efficient systems, advanced communications, high-bandwidth memory systems and intelligent sensing, there is growing demand for technologies that can efficiently bridge the physical and digital worlds. While digital computing continues to scale, many of the key bottlenecks in next-generation systems increasingly reside in analog, mixed-signal, RF, photonic, sensing, and power domains.

Emerging applications such as AI inference, edge computing, autonomous and efficient systems, quantum computing, and advanced wireless communications require ultra-efficient power delivery, high-bandwidth communication, and advanced sensing and signal conversion. Unlike digital scaling, these domains often face fundamental physical limitations related to energy efficiency, thermal constraints, signal integrity, materials limitations, physical form (e.g. size and weight), system integration complexity and supply chain resilience. As a result, advances in Analog & Mixed-Signal (AMS) technologies are becoming increasingly important enablers of future semiconductor systems.

Significant gaps, constraints, and challenges remain in advancing Analog & Mixed-Signal (AMS) technologies needed to support next-generation semiconductor systems. As applications mentioned previously continue to grow, semiconductor systems increasingly depend on efficient interaction between the physical and digital domains. However, analog, RF, photonic, sensing, and power technologies do not scale as efficiently as digital CMOS and are increasingly constrained by noise, variability, thermal limitations, signal integrity, and energy efficiency challenges. Existing design methodologies, modeling tools, and process technologies are often insufficient to support highly heterogeneous integration across advanced digital, analog, RF, photonic, and sensing components. In addition, emerging operating environments such as cryogenic systems and sub-THz / THz-frequency communications introduce new device behaviors, reliability concerns, packaging challenges, and limited availability of validated design infrastructure. These challenges are further compounded by growing requirements for hardware security, including resilience to side-channel attacks (power, electromagnetic, and fault-injection techniques) targeting cryptographic, post-quantum cryptographic, and AI model implementations, where analog and mixed-signal behaviors can create new vulnerabilities and attack surfaces.

Efficiently translating advanced AMS research into robust, manufacturable, and cost-effective products especially when market product is experiencing significant time and cost compression is critical. High volume analog and mixed signal solutions particularly in industrial, automotive, and infrastructure applications require strong emphasis on long term reliability, operation across wide environmental and process variations, and compliance with functional safety requirements. Academic research is encouraged to place emphasis on high-yield design, manufacturability, testability, calibration, and scalable validation methodologies required for commercial deployment. Furthermore, improving standardized approaches for analog IP reuse, design portability across process nodes, and lifecycle management will help

reduce barriers to rapid deployment and commercialization. Addressing these gaps is essential to enable practical, deployable AMS systems that meet real-world product constraints.

Future semiconductor systems also face growing constraints associated with power delivery, data movement, thermal management, and real time sensing and decision making. AI datacenters, edge devices, autonomous platforms, and high bandwidth communication systems require substantial improvements in power management, advanced packaging, photonic integration, sensor fusion, and low latency processing. At the same time, emerging technologies such as quantum transduction, embodied AI systems, autonomous physical systems, AI-enabled robotics, and cyber-physical intelligence, and RF-to-THz systems require advances in materials, architectures, devices, circuits, and system co-design approaches that are not yet mature. Progress is further limited by gaps in design automation, manufacturability, scalable integration methods, and cross-disciplinary workforce expertise. Equally important is the development of methodologies that bridge early-stage AMS research with production-scale deployment, including design-for-test, design-for-reliability, and cost-aware design optimization frameworks aligned with high-volume manufacturing requirements. Addressing these challenges will require exploratory and precompetitive research focused on developing new approaches to heterogeneous integration, energy-efficient architectures, advanced materials and devices, and tightly coupled hardware-software-physical system co-design.

## 1.4.2 Topic 2: Advanced Packaging

### Subtopics of Interest:

- Packaging architectures and codesign (w/System Architecture input)
- Packaging for Cryogenic environments
- Next generation interconnects
- Power delivery and thermal management
- Substrates and materials
- Heterogeneous integration: devices, processes, & materials
- Modeling and model validation
- Co-Packaged Optics (CPO)
- Security for packaging & HW design

### Background, Gaps, Constraints, and Challenges Addressed

Advanced packaging has become a critical technology driver for the semiconductor industry as traditional transistor scaling alone is no longer sufficient to deliver the performance, bandwidth, power efficiency, and system functionality required for emerging applications such as AI infrastructure, autonomous smart and secure systems, high-performance computing, and advanced wireless communications. Increasingly, system level performance improvements depend on integrating multiple heterogeneous devices, chipllets, memory technologies, photonics, sensors, and specialized accelerators into tightly coupled package architectures. As a result, advanced packaging is evolving from a backend assembly function into a primary system architecture and technology integration challenge requiring coordinated co-design across devices, circuits, packaging,

interconnects, thermal management, power delivery, secure heterogeneous integration, trusted packaging, hardware-rooted security, and tamper-resistant system architectures optimization for traditional, wafer-to-wafer, die-to-wafer, and die-to-die approaches.

Significant gaps and challenges remain in the development of scalable packaging architectures, heterogeneous integration approaches, and next generation interconnect technologies. Future systems require the ability to integrate components manufactured across different process nodes, materials platforms, and operating environments while maintaining signal integrity, reliability, manufacturability, and cost effectiveness. Existing packaging approaches face growing limitations associated with bandwidth density, latency, interconnect scaling, electromagnetic interference, mechanical stress, package warpage, and reliability under increasingly demanding thermal and power conditions. In parallel, co-packaged optics and photonic integration create both new opportunities and challenges involving optical-electrical integration, coupling efficiency, alignment precision, thermal sensitivity, and scalable manufacturing.

Power delivery and thermal management are also emerging as major system bottlenecks for advanced semiconductor platforms. AI accelerators, dense chiplet-based architectures, and high-bandwidth memory systems are driving unprecedented increases in power density and localized thermal loading. Existing package-level power distribution networks are increasingly constrained by IR drop, noise coupling, current delivery limitations, and cooling inefficiencies. Addressing these challenges will require advances in substrate technologies, advanced materials, thermal interface solutions, advanced package power delivery networks, silicon-package co-optimized power delivery architectures, and emerging backside power delivery technologies, embedded cooling concepts, integrated electro-thermal co-design methodologies. At the same time, future packaging systems must support higher levels of integration while maintaining reliability, yield, manufacturability, and long-term operational stability across diverse applications and operating environments.

Progress in advanced packaging is further constrained by gaps in modeling, simulation, design automation, and validation infrastructure. Current tools often lack the fidelity and interoperability needed to accurately predict behavior across highly heterogeneous multi-physics systems involving electrical, thermal, optical, mechanical, and material interactions. Validation methodologies, standards, and scalable test approaches remain immature for many emerging packaging technologies, particularly in areas such as chiplet ecosystems, co-packaged optics, cryogenic systems, and heterogeneous material integration. In addition, the increasing complexity of advanced packaging requires stronger collaboration across traditionally separate disciplines including semiconductor devices, materials science, photonics, circuit design, system architecture, manufacturing, and reliability engineering. Addressing these challenges will require exploratory and precompetitive research focused on new packaging architectures, integration methodologies, advanced materials, scalable interconnect technologies, predictive modeling capabilities, and holistic system package co-design approaches. Some examples are given below.

Photonics Integration for AI Systems can target co-packaged optics, photonic chiplets, embedded photonics, micro-LED. VCSEL based source integration and glass/polymer waveguide-RDL platforms, with emphasis on scalable assembly and optical interconnect reliability. Hybrid Bonding for heterogeneous integration can explore sub-micron die/wafer bonding,

low-temperature processes, yield improvement, and advanced metrology for defect control. Reliability of advanced packaging systems address AI/HPC-scale packages, including hybrid bonding interfaces, glass-based substrates, and predictive, data-driven reliability models. Advanced materials for Next-Gen Packaging focuses on glass and polymer substrates, high-performance thermal materials, bonding metallurgy (e.g., engineered Cu), and sustainable materials solutions. Finally, scalable manufacturing and process integration emphasizes optimized panel-level packaging, additive and laser-based processes, AI-driven manufacturing optimization, and tightly integrated thermal and process co-design to enable high-volume, high-yield production of next-generation heterogeneous systems.

The emergence of chiplet-based architectures has galvanized the industry to address critical challenges such as ecosystem development, interoperability standards, known-good-die (KGD) availability, capacity and scalable test and validation methodologies across multi-vendor components. At the same time, manufacturing readiness and supply chain scalability remain constrained by the imbalance between demand and availability of materials infrastructure, advanced assembly equipment, process integration capabilities, and the coordination of foundries, OSATs, and system integrators. Effective deployment of advanced packaging approaches can help ease the pressure on capability and capacity, create modular approaches, and improves efficiency through innovative redeployment of processes and structures. This will require improved methodologies for system-level design partitioning and System Technology Co-Optimization (STCO), including trade-offs between performance, latency, power, area, and interconnect complexity across heterogeneous components without sacrificing uptime reliability. Testing and validation, in particular, represent a major barrier to commercialization, as current approaches struggle with die-level versus package-level validation trade-offs, limited observability after assembly, and the absence of standardized embedded test structures for heterogeneous systems. Fault isolation in 2.5D and 3D integrated architectures is increasingly difficult due to dense interconnects and multi-layer integration, while system-level yield is further degraded by defect compounding across chiplets, interconnects, and assembly processes. In addition, efficient burn-in and reliability screening methodologies for complex heterogeneous systems remain underdeveloped. Furthermore, the economic viability of these approaches needs to be significantly improved as cost models must account for yield compounding, test complexity, assembly costs, and lifecycle reliability, all of which impact return on investment and adoption decisions. Addressing these ecosystem, design, and cost-related barriers will be essential to enable scalable, interoperable, and commercially viable advanced packaging solutions for next-generation semiconductor systems.

### 1.4.3 Topic 3: Manufacturing & Device Technology

#### Subtopics of Interest:

- Manufacturing process innovation, including AI-driven automation and robotics
- Materials and devices innovation (e.g., alternative channels, novel interconnects, functional BEOL)
- Patterning (e.g. high NA EUV materials & patterning innovation) and atomic scale processes (e.g. ALD/ALE & ASD)
- Manufacturing metrology and failure analysis
- Sustainable manufacturing (e.g., GWP gases, PFAS, Water recycling, effluent minimization & sustainable chemistries)
- Quantum- adjacent including Josephson Junctions

### **Background, Gaps, Constraints, and Challenges Addressed**

Manufacturing and device technology innovation remains foundational to the continued advancement of the semiconductor industry as emerging applications such as AI infrastructure, advanced communications, autonomous systems, quantum technologies, and high-performance computing drive unprecedented requirements for performance, power efficiency, bandwidth density, and heterogeneous integration. As traditional transistor scaling becomes increasingly difficult and expensive, future progress will depend on innovations across manufacturing processes, materials systems, device architectures, interconnect technologies, and advanced integration methodologies. Continued scaling and system advancements require breakthroughs in areas such as alternative channel materials, novel interconnect structures, functional BEOL integration, advanced interconnect architectures, and emerging backside power delivery networks, advanced patterning technologies, atomic-scale manufacturing processes, and highly precise process control. At the same time, increasing process complexity, manufacturing cost, and sustainability pressures are reshaping priorities across semiconductor fabrication ecosystems.

Significant gaps and challenges exist in extending manufacturing and device technologies beyond conventional CMOS scaling approaches. Advanced device architectures increasingly face limitations associated with electrostatics, variability, leakage current, thermal dissipation, interconnect resistance, and manufacturability at nanometer and atomic dimensions. Emerging materials and device concepts introduce additional integration complexity, reliability concerns, defect sensitivity, and compatibility challenges with existing semiconductor process flows. Patterning technologies, including high-NA EUV lithography and next-generation resist materials, must address shrinking process margins, stochastic defects, line edge roughness, overlay accuracy, and escalating process costs. Similarly, atomic-scale processes such as atomic layer deposition (ALD), atomic layer etching (ALE), and area-selective deposition (ASD) require improved precision, selectivity, throughput, and process integration to enable future device scaling and heterogeneous architectures.

Manufacturing metrology and process control also represent critical challenges as semiconductor fabrication approaches atomic-scale dimensions and increasingly heterogeneous integration environments. Existing metrology techniques often lack sensitivity, speed, spatial resolution, or in-line capability needed to characterize complex and assembled three-dimensional structures, buried interfaces, advanced materials systems, and stochastic process variations. The growing complexity of advanced manufacturing flows requires improved multi-physics modeling, real-time sensing, predictive process control, defect detection, and digital manufacturing methodologies capable of supporting high-yield, high-volume manufacturing. In addition, quantum-adjacent technologies, including Josephson junctions and superconducting device structures, introduce new challenges related to materials purity, cryogenic operation, interface control, process variability, and scalable fabrication approaches that are not yet fully mature.

The semiconductor industry also faces increasing pressure to improve sustainability and reduce the environmental impact of manufacturing operations to ensure that their new facilities can be good neighbors. Advanced semiconductor fabrication consumes substantial amounts of energy, water, specialty chemicals, and high-global-warming-potential (GWP) gases while generating complex waste streams and effluents. Growing regulatory, environmental, and supply chain pressures are driving demand for sustainable manufacturing approaches including PFAS reduction and replacement, water recycling, effluent minimization, lower-emission process chemistries, and more resource-efficient manufacturing techniques.

Addressing these combined challenges will require exploratory and precompetitive research focused on next-generation materials and devices, atomic-scale process technologies, advanced metrology and process control, scalable quantum-adjacent manufacturing, and sustainable semiconductor manufacturing solutions capable of supporting future industry growth and global competitiveness.

## 2. Proposal Submission Process

All proposals must be submitted through SRC's web-based proposal management, OpenWater. The following sections outline required elements for a submission, formatting guidelines for all elements, guidance on proposal content, and budgeting guidance.

This is a collaborative, two-round solicitation process. The first round requires submission of a concept paper. Selected applicants will be invited to submit a full proposal in the second round.

### 2.1 Required Concept Paper Elements

Concept papers serve as preliminary proposals that allow applicants to present their ideas concisely before investing significant resources in a full proposal. They help enable the program industry members to review and quickly select applicants to be invited for full proposal. Following review of the Concept Papers, submitters will either be invited to develop and submit a Full Proposal or will not advance to the proposal stage. For those invited to submit a Full Proposal, reviewers may provide limited feedback to strengthen alignment with program objectives, technical merit, and project viability. This feedback is intended to help applicants refine their proposed approaches and, where appropriate, redirect efforts to better address program priorities.

The two-page concept paper must address the following elements. While section headers are not mandatory, applicants should ensure all required information is clearly presented.

**Table 1. Required Concept Paper Elements**

<p><b>I. Background and Need</b> <b>a. Alignment with Program Goals</b></p>	<p>Clearly describe the technical problem, gap, or opportunity the proposed work will address, and explain why it is novel, innovative, significant and timely. Provide sufficient context to demonstrate understanding of the current state of knowledge, gaps or practice in the relevant field.</p> <p>This section should articulate what problem(s) are being solved, why they matter, and how the proposed approach advances the field.</p> <p>Applicants must also explicitly describe how the concept aligns with the objectives, focus areas, and priorities outlined in the solicitation. Reference relevant technical areas, application domains, or programmatic themes to demonstrate alignment with program goals and intent. Identify if related to any previous SRC program work.</p>
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<p><b>II. Proposed Approach</b> <b>a. Expected Impact and Outcomes</b></p>	<p>Describe the technical approach or methodology that will be used to address the identified challenge. Clearly explain how the proposed work will be executed, including the scientific or engineering rationale for why the approach is expected to succeed. Highlight what is novel or innovative compared to existing solutions or prior research, and summarize the key technical tasks, phases, or objectives. Define the anticipated results, deliverables, and outcomes of the project, including how success will be measured. Describe the tangible outputs (e.g., data, models, prototypes, or methodologies) and the expected impact on the relevant field, industry, or application domain. Address both near-term deliverables and longer-term implications and summarize the top 2–3 milestones that will indicate progress and success. Highlight industry ecosystem leaders, particularly SRC members that will directly benefit from the outcomes.</p>
<p><b>III. Team Qualifications and Resources</b></p>	<p>Briefly describe the unique qualifications of the team or organization to successfully complete the proposed work. Highlight relevant expertise, prior accomplishments, unique facilities, or strategic partnerships that position the team for success. If collaborations are proposed, explain the role of each partner and the value they bring to the project.</p>
<p><b>IV. Budget and Timeline</b></p>	<p>Provide a budget estimate for the proposed work, including the total project cost and major cost categories if relevant. Indicate the proposed project duration. Detailed budget justification is not required at this stage, but the estimate should be realistic and commensurate with the proposed scope of work and in line with the project budgets outlined in this document</p>

Concept Papers will be accepted online at: [Landing Page](#)

The deadline for receiving concept papers is 11:59 PM EASTERN TIME on 06/30/2026.

## 2.2 Concept Paper Format Guidelines

### Length and Format

Concept papers contents must not exceed two (2) pages, this excludes a cover page and a singular reference page, if used. Highlight any SRC sponsored work on the reference page. The two-page limit is strict and will be enforced. Pages exceeding this limit will not be reviewed.

**All submissions must adhere to the following formatting requirements:**

- **Figures, Graphs, Images, and Pictures**
  - Figures and tables must be numbered and referenced in the text by that number. They should be of a size that is easily readable and may be in landscape orientation. They must fit on an 8.5 by 11-inch paper size.



- **Font**
  - The concept paper should use easy-to-read font (such as Times New Roman or Arial, 10-point minimum), single spaced. Smaller font may be used in figures and tables but must be legible. Images generated using AI should be marked as such.
- **Page Layout**
  - The concept paper must be in portrait orientation except for figures, tables, graphs, images, and pictures. Pages shall be single-spaced, 8.5 by 11-inches, with at least one-inch margins on all four sides of each page.
- **Page Limit**
  - The concept paper is limited to 2 pages, the cover page and reference page are not included in the 2 page limit. Pages that exceed these guidelines may not be reviewed.
- **Page Numbering**
  - Number pages sequentially, excluding the cover page.
- **File Type**
  - File must be submitted as a .PDF
- **Cover Page (Optional, Not Counted Toward Page Limit)**
  - If included, the cover page should contain:
    - Concept paper title
    - Technical Tracks addressed
    - Track Lead's name, title, organization affiliation, email, and phone number
    - Collaborating organizations (if applicable), number of projects, and project leads
    - Estimated budget including cost share
    - Date of submission

**PDF file name format should be: *Abbreviated Proposal Title; Track Lead Last Name; Track Lead First Name***

## 2.3 Required Full Proposal Elements

A complete full proposal shall consist of organizational information submitted through OpenWater:

- **Technical Narrative:** A comprehensive document that includes an Executive Summary; Background and Need; Technical Objectives, Scope, and Approach; and the Workplan including Milestones, Budget Justification, and Cost Share.
- **Summary PowerPoint Slide:** A single slide that provides a high-level overview of the project's budget, funding, duration, objectives, and key deliverables for quick review.
- **Consolidated Track Budget Workbook:** For the entire proposal inclusive of all projects, supplying detailed cost calculations that complement the high-level budget summary included in the Technical Narrative.
- **Budget Workbook per Project (1-3):** A detailed Excel spreadsheet that breaks down all project(s) costs including labor, materials, travel, overhead, and cost-sharing requirements by organization and funding source.

Required templates for the PowerPoint Slide, Budget Workbook, are available for download online at: [Landing Page](#)

The deadline for receiving invited full proposals is 11:59 PM EASTERN TIME on 09/14/2026.

### 2.3.1 Full Application Narrative Content Guidelines

The proposal table of contents and guidelines are provided in this section. The Technical Narrative must not exceed 15 pages in total, excluding appendices. While suggested page counts are provided for each section as guidance, they are flexible, what matters most is that the overall narrative stays within the page limit.

Technical Narrative Content – 15-Page Maximum for Sections 1-5	
Suggested Length	Section and Contents Note
	Cover pages, table of contents, references, and glossaries are not included in the page count
~2 pages	1. Executive Summary 1.1. A succinct summary of no more than two pages clearly articulating the big picture problem being addressed, proposal objectives, approach to address all critical technical and non-technical aspects, expected outcome and overall cost/cost share information.
~2 Pages	2. Background and Need 2.1. Identify the opportunity and proposed solution 2.2. Describe background, current state-of-the-art, and alignment to Technical Topics. Highlight if two or more Technical Topics are covered. 2.3. Address <a href="#">MAPT Roadmap</a> Gap (or gap not previously identified) and problem definition 2.4. Summarize novelty, innovation, and how this will efficiently close the gap 2.5. Identify if related to any previous SRC program work.
~5 Pages	3. Technical objectives, scope, and approach 3.1. Technical objectives 3.2. Technical scope and approach 3.3. Innovative claims 3.4. Performance and reliability metrics/standards, alignment with solicitation objectives 3.5. Identify why it is relevant to program member companies 3.6. Key target deliverables (see paragraph below)
~4 Pages	4. Work plan 4.1. Project schedule 4.2. Detailed description of milestones, tasks, and deliverables 4.3. Project management approach, roles of key personnel
~2 Pages	5. Budget justification and costs 5.1. Summary breakdown of costs (labor, materials, travel, etc.) by project team member. Sources of funding include SRC funds, participant cost share, third-party cost share, and any other sources. This section provides budgetary information for technical reviewers.

**Key Target Deliverables:** Please ensure that proposals clearly identify the current capability and the Specific, Measurable, Achievable, Relevant, and Time-Bound (S.M.A.R.T.) Key Target deliverables that will determine the project's success. Proposals must define milestones that are tangible, measurable, or demonstrable. The deliverables of each milestone achievement should be clearly defined as well as the starting state of the art for the same characteristics that the project is improving upon. Examples of tangible milestone deliverables may include physical samples, written reports containing collected data, or live demonstrations of functionality.

### 2.3.2 Cost Proposal Guidelines

Each proposal must submit cost calculations for each project and shall be in the Excel format provided; spreadsheet(s) should be submitted as a separate file with the submission. For clarity, Section 5 of the Technical Narrative includes a high-level budget summary that technical reviewers will use to evaluate the proposal.

The budget workbook template may be downloaded at [Landing Page](#). Additional worksheets should be added to the Workbook for additional subcontract partner organizations.

Cost proposals must include labor (by staff position/role, not by individual name), materials, travel, and all other direct expenses, and overhead, including overhead rates, each divided by source of funds. Questions about cost proposals, including submission of rate information, should be addressed to SRC at [proposals@src.org](mailto:proposals@src.org)

### 2.4 Full Proposal Format Guidelines

The proposer shall submit one (1) electronic copy of their proposal package via online submission form at: [Landing Page](#). The proposal package consists of the files outlined in Section 2.3. To maintain consistency through submission, review, and approval processes, please follow the guidelines below.

#### Technical Narrative

- **Figures, Graphs, Images, and Pictures**

- Figures and tables must be numbered and referenced in the text by that number. They should be of a size that is easily readable and may be in landscape orientation. They must fit on an 8.5 by 11-inch paper size.

- **Font**

- Proposals are to be prepared with easy-to-read font (such as Times New Roman or Arial, 10-point minimum), single-spaced. Smaller font may be used in figures and tables but must be legible.

- **Page Layout**

- The proposal document must be in portrait orientation except for figures, tables, graphs, images, and pictures. Pages shall be single-spaced, 8.5 by 11-inches, with at least one-inch margins on all four sides of each page.

- **Page Limit**

- The Technical Narrative is limited to a maximum of 15 pages. Proposals that exceed these guidelines will not be reviewed.

- **Page Numbering**
  - Number of pages sequentially within each major section of the proposal (front matter, proposal content, appendices).
- **File Type**
  - File must be submitted as a .PDF
  - PDF file name format should be: Abbreviated Proposal Title; Track Lead Last Name; Track Lead First Name

#### **Summary PowerPoint Slide**

The Summary PowerPoint Slide must be submitted using the template provided by SRC [Landing Page](#). Each project is required to provide a single PowerPoint slide for their proposal which covers the 5 topics in the technical narrative content that outlines the proposed budget, objective, and top (2-3) milestones, to be used while reviewing and selecting proposals. Graphics or other relevant and impactful materials are often helpful in this regard. Proposals that are selected for funding will be required to provide a version of this slide for public release as part of the contracting process.

#### **Budget Workbook**

The Consolidated Track Budget Workbook (for entire proposal including all projects) must be submitted using the official template provided by SRC. This spreadsheet is designed to supply detailed cost calculations that complement the high-level budget summary included in the Technical Narrative. The completed workbook must present a comprehensive and itemized breakdown of all project costs, organized by funding sources including federal funds, the required minimum 20% cost share, and any third-party contributions. Both PDF and Excel versions are required to be submitted.

#### **You must utilize your lowest government approved indirect cost rate when preparing the budget.**

In addition to the Consolidated Track Budget Workbook, an individual Budget Workbook must be completed and submitted for each project to ensure accuracy, compliance, and proper allocation of resources. Both PDF and Excel versions are required to be submitted.

## **3. Project Administration**

### **3.1 Cost-Sharing Requirements**

All projects must have a minimum 20% cost share. Higher cost share is welcome but not heavily weighted as selection criteria.

### **3.2 Financial Tracking Requirements**

Project agreements will be awarded as cost reimbursement, not-to-exceed contracts, with a quarterly invoicing requirement. If the proposer's organization has a U.S. government-approved rate structure, it must be used. Note that Commercial rates or profit (fee) are not allowable for Project Solicitation proposal submissions.

All proposers are expected to have a government approved or industry standard accounting system by which actual project costs are tracked and reported. This is a requirement to ensure that cost share obligations are met. The methods used to value "cost sharing" must be the same as those used to value the full project costs.



### 3.3 Contracting of Selected Proposals

Funded proposals will be supported through cost-reimbursement contracts executed under SRC's Sponsored Research Agreement (SRA). Proposals may include up to three collaborating projects. However, each project will be awarded and administered under a separate contract. Cost reimbursement payments will be made quarterly based on submitted invoices. An example of the typical terms and conditions, including IP rights and other key elements for a Sponsored Research Agreement, can be found here: [Landing Page](#)

The Contractor (research entity) retains exclusive ownership of all foreground IP created during the project. The Contractor grants SRC an irrevocable, royalty-free, worldwide, nonexclusive license to all foreground IP (including the right to make, use, sell, reproduce, and distribute inventions and works of authorship) and SRC may sublicense those rights to its member companies (and their end users, OEMs, and suppliers). Background IP owned by the Contractor that blocks or would necessarily be infringed by use of the foreground ("Implicated Background") must be disclosed prior to contract start and Contractor shall grant SRC and Members a non-exclusive, royalty-free license for limited use of the Implicated Background to permit the scope of activities allowed under the foreground IP license. Additional information regarding SRC's intellectual property policies can be found at the following link: [IP Policies](#).

For proposals selected for funding, awardees will be expected to provide reports on project progress and performance outcomes. In addition to meeting the project milestones set forth in the proposal, this may include, for example, annual scorecard updates and documentation of technology transfers to member companies, as tracked through SRC's [Key Performance Indicator \(KPI\)](#) system.

## 4. Concept Paper Review and Evaluation Process

### 4.1 Concept Paper Review Process

SRC employs a multi-stage review process to ensure the best portfolio of proposals is selected for meeting the objectives of this solicitation.

#### Concept Paper Review Process

1. **Administrative Review** SRC staff screen all submitted concept papers for compliance, completeness, and eligibility before they advance to technical evaluation.
2. **Technical Merit Review** Subject matter experts at SRC SPARC program member companies evaluate each concept paper for alignment with industry interests, assessing the proposed approach, objectives, work plan, and budget justification.
4. **Concept Paper Decisions** Industry program members collectively review concept papers to determine which will be invited to submit full proposals. Selection is not based solely on technical merit, but additional factors include balance across priority technical topics, the number and enrollment type of students supported and trained throughout the project, and relevance to program members' strategic interests.

5. **Notifications** SRC will notify all submitters of the outcome. Limited feedback may be provided where available from reviewers.

## 5. Full Application Review and Evaluation Process

### 5.1 Proposal Review Process

SRC employs a multi-stage review process to ensure the best portfolio of proposals is selected for meeting the objectives of this solicitation.

#### Full Proposal Review Process

1. **Administrative Review:** SRC staff screen all submitted proposals for completeness and eligibility before they advance to technical evaluation.
2. **Technical Merit Review:** Subject matter experts at SRC SPARC member companies evaluate each proposal against established criteria, providing written assessments and ratings.
3. **SRC Review:** SRC synthesizes reviewer assessments and evaluates overall portfolio balance, then develops selection recommendations. Note that these recommendations go beyond evaluation scores alone, additional considerations include balance across priority technical topics, the number of students supported and trained throughout each project, and alignment with program members' strategic interests.
4. **Research Council (RC) Review:** The Research Council reviews the synthesized assessments and portfolio balance evaluation, then makes final project selection decisions.
5. **Award Notification:** SRC notifies all proposers of award decisions.
6. **Award Negotiation and Contracting:** Selected proposals (tracks) begin Sponsored Research Agreement contracting. SRC will contract with each project lead's organization separately for each project under the track according to SRC standard terms and conditions [Landing Page](#). This process must be completed by January 1, 2027, with research commencing on that date.

### 5.2 Merit Review Evaluation Criteria

Full proposals will be evaluated on their overall scientific and technical merit and to the degree to which they advance the objectives of this solicitation. Evaluations will be based on the following weighted criteria:

#### Criteria 1: Technical Innovation & Potential (Weight 20%)

Is the work genuinely new and potentially transformative? How far does this move the field forward globally?

- To what extent does the proposal introduce novel concepts, architectures, materials, or approaches beyond incremental improvements?
- Does the work challenge existing paradigms or open new technical directions for the semiconductor ecosystem?
- Is innovation clearly articulated and differentiated from prior art?
- If successful, would the work represent a meaningful advance beyond current global capabilities?
- Does the proposal articulate quantifiable or clearly defensible performance gains?



- Is the advancement compelling relative to international competitors and benchmarks?

**Criteria 2: Technical Impact (30% Weight):**

- Will this make a difference to program industry members if it's successful? What is the payoff if this succeeds?
- Does the research focus on exploratory, fundamental, or applied research at early stages of technological maturity, well before the development phase, with the goal of identifying and validating promising research pathways?
- Does the project have the potential to enable breakthroughs in semiconductor technology?
- Could the outcomes significantly influence design, manufacturing, packaging, reliability, or system performance to help accelerate scalability?
- Is the impact clearly articulated and relevant to industry needs?

**Criteria 3: Technical Soundness and Project Methodology (Weight 10%)**

Is this the right plan? Does the team understand the problem and its challenges?

- Does the proposal demonstrate a clear understanding of the current state-of-the-art?
- Are key technical risks, limitations, and challenges identified and realistically assessed?
- Are assumptions well-founded and supported by data, theory, or prior results?
- Are the proposed methods technically sound and appropriate for the stated objectives?
- Does the proposal effectively apply proven techniques in new contexts, or introduce novel methods with solid theoretical grounding?
- Are milestones, experiments, and validation approaches well defined?

**Criteria 4: Teaming and Execution Capability (Weight 10%):**

Is this the right team? Can this team deliver?

- Does the team have the right expertise, roles, resources, and balance to execute the work?
- Are students meaningfully involved in technical work? General guidance is that each Project within the Technical Track proposal should be led by a faculty with teams of 2- 3 students of various degree levels pursuing a shared agenda.
- Is there a clear plan for mentorship, skills development, and training?
- How much does the proposal strengthen the future semiconductor talent pipeline?
- Are responsibilities clearly defined across partners?
- Is there evidence of prior success in similar or relevant projects?

**Criteria 5: Budget Considerations (Weight 30%)**

Is this the right budget? Is the project financially realistic and efficient?

- Is the proposed budget realistic and well-aligned with the scope of work?
- Are costs reasonable relative to expected outcomes and impact?
- Does the proposal meet or exceed minimum required cost share contributions?



## 6. Conclusion

The launch of SPARC (Semiconductor and Packaging Advanced Research Consortium) represents an exciting milestone for SRC's projects-based program and the semiconductor ecosystem. As outlined in the program guidance, SPARC creates an industry-driven framework that aligns academic research closely with real world needs, enabling faster translation of ideas into impactful outcomes.

By connecting early-stage research with industry priorities, SPARC is positioned to accelerate semiconductor innovation, delivering novel, innovative ideas but with an eye on practical outputs in order to reduce the gap between discovery and commercialization. At the same time, it plays a critical role in developing next-generation talent by immersing students in hands on, industry relevant research experiences.

SRC extends our deep appreciation to the SPARC Research Council, made up of representatives from SPARC member companies. Their leadership, commitment, and vision have established the strong foundation that made the launch of this program possible. We also thank our academic partners, whose pioneering research continues to advance innovation and create meaningful impact. Together, the SPARC community is fostering sustained collaboration, accelerating technical progress, and driving long-term impact across the semiconductor ecosystem.