'*' indicates required field
? indicates online help

29th Xcelerator Technology Innovation Awards

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Disclaimer

29th Xcelerator Technology Innovation Awards

By participating in the Xcelerator contest, you warrant that your Submission is your own original work, created solely by you. For the purposes of this contest, "Submission" shall mean the work provided to Siemens, such as textual and graphical descriptions of a product, and not the actual product. By entering this contest you acknowledge and agree that Siemens AG, at its discretion, may publish any part of your Submission, including, but not limited to, screen shots and images of the design, your name and your company or school affiliation. Siemens AG may publish this information when disclosing winners, in press releases, on web sites, in presentations or in any other promotional publication. Siemens AG is not responsible for any lost or misplaced submissions.

Disclaimer response *

☐ Accept

Contact

If you have questions about the Xcelerator Technology Innovation Awards or design entry process, please contact the administrators at pcb_tla@mentor.com.

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First name *

Last name *

Email address *

Company name *

Mentor/Siemens contact

Design category *

(select)

Industry *

Select

Design name *

End-product description *

Unique features * ?

Critical constraints * ?

Intended use of the submitted design version *

○ Proof of concept ○ Low-volume production ○ High-volume production

Tool flow *

○ Xpedition Enterprise ○ PADS Professional ○ PADS Standard/Plus ○ Board Station ○ Other

Tools used * ?

Units *

- (•) Imperial (th)
- ( ) Imperial (in)
- ( ) Metric (um)
- ( ) Metric (mm)

Smallest grid-array pin pitch * ?

[ ] th

High-speed nets (%) * ?

[ ]

Number of voltage rails * ?

[ ]

Number of ground nets *

[ ]

Placement density *

Select

Routing density *

Select

Swappable I/Os * ?

[ ]

Board thickness *

th

Total metal layers *

Layer stack-up * ?

Choose File No file chosen

Stack-up definition * ?

Fastest data rate (gbps) * ?

Signal integrity concerns * ?

EMI/EMC shielding concerns * ?

EM field effect concerns * ?

Power distribution network concerns * ?

Thermal concerns * ?

Verification tool usage * ?

Trace Width/Spacing

Minimum width * ?

th

Minimum spacing *

th

Typical width * ?

th

Typical spacing *

th

Via Size

Minimum hole size * ?

th

Typical hole size * ?

th

Percent nets testable after assembly *

Number of nets testable after assembly *

Packaging technologies ?

- [ ] Printed electronics
- [ ] Package design
- [ ] Embedded components
- [ ] Buried resistance
- [ ] Etched RF components
- [ ] Flex/rigid-flex

DfX ?

- [ ] Producibility
- [ ] Reliability
- [ ] Quality
- [ ] Cost

Size of design team * ?

Design team functions * ?

Total calendar time (weeks) * ?

Architecture definition time (weeks) *

Schematic design time (weeks) *

Layout design time (weeks) *

Verification time (weeks) *

Manufacturing prep time (weeks) *

How did you collaborate with Mechanical? * ?

How did you collaborate with Manufacturing? * ?

Schematic / layout iterations * ?

Layout / mechanical iterations * ?

Layout / manufacturing iterations * ?

IPC performance class * ?

Select

Additional comments ?

Attachments

Please attach any files related to your design. You may combine multiple files into one or attach up to three files separately. Alternatively, you can add a comment with an FTP address or request contact to upload.

File 1 * ?

Choose File No file chosen

File 2

Choose File No file chosen

File 3

Choose File No file chosen

Fabrication drawing * ?

Choose File No file chosen

Representative image * ?

Choose File No file chosen

Comments about attachments